# LOSSES DISTRIBUTION IN THREE-LEVEL VOLTAGE SOURCE INVERTERS 

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#### Abstract

Static converters design has to guarantee that in all specific operating conditions the junction temperature of power devices does not exceed admitted limits. The temperature of different components depends on losses distribution and on the number of switches in IGBT modules. This paper investigates the losses balancing in the most popular 3L conversion structures: 3L-Stacked Cells, 3L-Neutral Point Clamped (NPC) and 3L-Active NPC. The 3L-Active NPC concepts accomplish a two independent stages conversion which leads to a better equilibration of losses. The 3L-Stacked Cells topology was experimentally realized and some results are presented in the paper.


Keywords: Multilevel converters, Voltage source converters, Losses balancing, Pulse width modulation.

## 1. INTRODUCTION

Multilevel structures have been studied for over 25 years and they represent an intelligent solution to connect serial switches [1]. There is a limited number of converters suitable for medium voltage applications which deliver multilevel voltages. The first developed topology has consisted in a serial connection of singlephase inverters with DC separate sources [2]. This structure was followed by a study concerning the stacked commutation cells in order to obtain a multilevel conversion (SC - Stacked Cells) [3]. The main source was made of many secondary sources serially connected. The first experimental results were published 18 years later [4]. Fig.1a shows a 3L-SC structure, which is also called "three-pole cell" [5].
Following the SC concept study, a new multilevel NPC (Neutral Point Clamped) structure was developed [6], [7]. This is the most popular multilevel conversion structure. The 3L-NPC inverters (Fig.1.b) are considered a particular way of implementing 3L-SC topology [5]. The role of the middle side in the 3L-SC structure is taken by the inner switches and by the two clamp diodes.
Later, another invention [8] introduced the concept of the multilevel converter with flying capacitors (FC Flying Capacitor, Fig.1c). In the field of low and
moderate frequencies ( $200 \mathrm{~Hz}-1 \mathrm{kHz}$ ) the NPC structure is more advantageous than the FC structure because of the required flying-capacitor size, which is inversely proportional to the switching frequency.
Recently, the 3L-NPC structure performances were improved by developing the 3L-ANPC (Active NPC) converter [9], [10] (Fig.1d). It allows a significant increase of the output power and improves performances at "zero" speed [11].
This paper calculates and compares losses in power devices between three popular topologies: 3L-SC, 3L-NPC and 3L-ANPC. The commutation cells are composed by IGBT modules type Eupec FF200R33KF2C, and the clamp diodes are equivalent to the IGBT modules' diodes. The analysis made on the $3 \mathrm{~L}-\mathrm{SC}$ and 3L-NPC topologies proved that the losses in middle side power devices (3L-SC) and the losses in clamp diodes (3L-NPC) increase simultaneously with the reducing of the modulation index. This leads to the increase of the junction temperature in power devices which limits the converters output power, especially at "zero" speed operation. The paper shows that 3L-ANPC structure leads to the best losses balancing in power devices.
The 3L-Stacked Cells topology was experimentally realized and some results are presented in the paper.


Fig.1. Popular 3L structures:
(a) 3L-SC, (b) 3L-NPC, (c) 3L-FC, (d) 3L-ANPC.

## 2. POPULAR 3L STRUCTURES

### 2.1. Stacked Cells Structure

The 3L-Stacked Cells structure (3L-SC) is made of 6 switches disposed on three sides (Fig.1a). Each switch is capable to support a voltage equal to $V_{D C} / 2$. The exterior sides are made of two switches serially connected and the middle side is composed by two switches opposite connected. The middle point of the two serial voltage supplies is defined as neutral point. The switches form 3 commutation cells controlled with $\alpha_{1}, \alpha_{2}$ and $\alpha_{3}$ duty cycles: cell $1\left(\mathrm{~S}_{1}-\mathrm{S}_{1 \mathrm{c}}\right)$, cell 2 $\left(\mathrm{S}_{2}-\mathrm{S}_{2 \mathrm{c}}\right)$ and cell $3\left(\mathrm{~S}_{3}-\mathrm{S}_{3 \mathrm{c}}\right)$. A sinusoidal PWM strategy was used in order to emphasize the constraints applied to $3 \mathrm{~L}-\mathrm{SC}$ converter (Fig.2).

The PWM strategy has four switching states (Table 1). The output voltage ( $v_{A O}$ ) has three states: $V_{D C} / 2,0$ and $-V_{D C} / 2$. Two switching states ( P and N ) correspond to direct connection of the load at DC voltage and the others states correspond to obtain " 0 " voltage level $\left(\mathrm{O}_{1}^{-}\right.$and $\left.\mathrm{O}_{2}{ }^{+}\right)$. For $V_{D C} / 2$ voltage level (P) the switches $\mathrm{S}_{1}, \mathrm{~S}_{2}$ and $\mathrm{S}_{3}$ must be turned on. For $-V_{D C} / 2$ level (N) the switches $\mathrm{S}_{1 \mathrm{c}}, \mathrm{S}_{2 \mathrm{c}}$ and $\mathrm{S}_{3 \mathrm{c}}$ must be turned on.


Fig.2. Duty cycles for 3L-SC and 3L-ANPC topologies.

The $\mathrm{O}_{1}^{-}$state is obtained when the reference output voltage is negative. In this case the $\mathrm{S}_{1 \mathrm{c}}, \mathrm{S}_{2 \mathrm{c}}$ and $\mathrm{S}_{3}$ are turned on. The $\mathrm{O}_{2}^{+}$state is obtained when the reference output voltage is positive. For this switch sequence the $\mathrm{S}_{1 \mathrm{c}}, \mathrm{S}_{2}$ and $\mathrm{S}_{3}$ must be turned on.

| Output <br> Voltage <br> $\left(v_{A O}\right)$ | Switching <br> State | Switch Sequence |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $S_{I c}$ | $S_{2}$ | $S_{2 c}$ | $S_{3}$ | $S_{3 c}$ |  |
| $-V_{D C} / 2$ | $N$ | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | $O_{1}{ }^{-}$ | 0 | 1 | 0 | 1 | 1 | 0 |
|  | $O_{2}{ }^{+}$ | 0 | 1 | 1 | 0 | 1 | 0 |
| $V_{D C} / 2$ | $P$ | 1 | 0 | 1 | 0 | 1 | 0 |

Table 1. Output voltage for the switching sequences of 3L-SC.

The energy conversion is based on two partial uncoupled stages and this represents a disadvantage for the structure. The middle side is common for the both energy conversion stages. This leads to the
increase of conduction losses in $\mathrm{S}_{1 \mathrm{c}}$ and $\mathrm{S}_{3}$ switches, which limit the load current, especially at low modulation index.

### 2.2. Neutral Point Clamped Structure

A three-level neutral point clamped structure (3LNPC) is shown in Fig.1b. The four switches form two commutation cells controlled by $\alpha_{1}$ and $\alpha_{2}$ duty cycles: cell $1\left(\mathrm{~S}_{1}-\mathrm{S}_{1 \mathrm{c}}\right)$ and cell $2\left(\mathrm{~S}_{2}-\mathrm{S}_{2 \mathrm{c}}\right)$. The duty cycles (Fig.3) are obtained by following a sinusoidal PWM strategy. The clamp diodes $D_{u}$ and $D_{d}$ are the distinct elements of this circuit. Compared to the 3LSC topology, this structure use only three switching states $(\mathrm{P}, \mathrm{O}$ and N ) to obtain the three voltage levels (Table 2). "O" switching state is obtained by turning on the inner switches ( $\mathrm{S}_{1 \mathrm{c}}$ and $\mathrm{S}_{2}$ ). In this case the load inductive current can pass through two different paths. If the load current is positive, it passes through the $D_{u}$ clamp diode and the $\mathrm{S}_{2}$ switch. If the load current is negative, the path is through the $\mathrm{D}_{\mathrm{d}}$ clamp diode and the $S_{1 c}$ switch.


Fig.3. Duty cycles for 3L-NPC topology.

| Output | Switching <br> Voltage <br> $\left(v_{A 0}\right)$ | Switch Sequence |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $S_{l}$ | $S_{I c}$ | $S_{2}$ | $S_{2 c}$ |
| $-V_{D C} / 2$ |  | 0 | 1 | 0 | 1 |
| 0 |  | 0 | 1 | 1 | 0 |
| $V_{D C} / 2$ |  | 1 | 0 | 1 | 0 |

Table 2. Output voltage for the switching sequences of 3L-NPC.

### 2.3. Active Neutral Point Clamped Structure

The 3L-ANPC structure was developed in order to obtain a better balancing of losses in power devices. An active switch is anti-parallel connected with clamp diodes from NPC structure (Fig.1d). The three commutation cells are controlled by $\alpha_{1}, \alpha_{2}$ and $\alpha_{3}$ duty cycles: cell $1\left(\mathrm{~S}_{1}-\mathrm{S}_{1 \mathrm{c}}\right)$, cell $2\left(\mathrm{~S}_{2}-\mathrm{S}_{2 \mathrm{c}}\right)$ and cell 3 ( $\mathrm{S}_{3}-\mathrm{S}_{3 \mathrm{c}}$ ).

The modification of duty cycles is made similarly to the 3L-SC topology (Fig.2) following a sinusoidal PWM strategy.

The switches are disposed on two independent stages: stage $1\left(\mathrm{~S}_{1}, \mathrm{~S}_{1 \mathrm{c}}\right.$ and $\left.\mathrm{S}_{2}\right)$ and stage $2\left(\mathrm{~S}_{2 \mathrm{c}}, \mathrm{S}_{3}\right.$ and $\left.\mathrm{S}_{3 \mathrm{c}}\right)$. The cell 1 and cell 3 switch at a high frequency while the cell 2 switches at a low frequency. Similarly to the 3L-SC structure, the PWM strategy for 3L-ANPC has four switching states (Table 3).

| Output <br> Voltage <br> $\left(v_{A O}\right)$ | Switching <br> State | Switch Sequence |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $S_{I c}$ | $S_{2}$ | $S_{2 c}$ | $S_{3}$ | $S_{3 c}$ |  |
| $-V_{D C} / 2$ |  | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 |  | 0 | 0 | 0 | 1 | 1 | 0 |
|  |  | 0 | 1 | 1 | 0 | 0 | 0 |
| $V_{D C} / 2$ |  | 1 | 0 | 1 | 0 | 0 | 0 |

Table 3. Output voltage for the switching sequences of 3L-ANPC.

The " 0 " voltage level is obtained by two switching states $\left(\mathrm{O}_{1}^{-}\right.$and $\left.\mathrm{O}_{2}{ }^{+}\right)$: Thus the load current can pass in both directions only through stage 1 (paths: $\mathrm{S}_{1}-\mathrm{S}_{2}$ or $\mathrm{S}_{1 \mathrm{c}}-\mathrm{S}_{2}$ ) or only through stage 2 (paths: $\mathrm{S}_{3 \mathrm{c}}-\mathrm{S}_{2 \mathrm{c}}$ or $\mathrm{S}_{3}-$ $\mathrm{S}_{2 \mathrm{c}}$ ).

## 3. LOSSES DISTRIBUTION

### 3.1. Calculus of Total Losses

The evolution of temperature in IGBT modules is a direct consequence of the total losses and imposes the maximum power that can be delivered by power switches.
The following hypotheses were considered to calculate the losses in power devices:

- all semiconductor devices switch at the same voltage, equal to $V_{D C} / 2$;
- the load is considered linearly;
- the load current is sinusoidal;
- the current and voltage ripples are neglected;
- the phase-shift $\theta$ between the load current $\left(i_{\text {load }}\right)$ and the output voltage $\left(v_{A O}\right)$ is included in $[0, \pi]$ interval;
- the dead times of the IGBT modules are neglected.

The total losses $\left(P_{X}\right)$ are made up of conduction losses ( $P_{\text {cond } X}$ ) and switching losses $\left(P_{s w X}\right)$ [12]:

$$
\begin{equation*}
P_{X}=P_{c o n d X}+P_{s w X} \tag{1}
\end{equation*}
$$

## A) Conduction losses

The conduction losses are obtained as a sum of all conduction losses in transistors ( $P_{\text {condT }}$ ) and diodes ( $P_{\text {condD }}$ ):

$$
\begin{gather*}
P_{\text {cond } X}=P_{\text {condT }}+P_{\text {condD }}  \tag{2}\\
P_{\text {cond } T}=v_{C E 0} \cdot I_{\text {avg }}^{c o n d T}+r_{d T} \cdot\left(I_{r m s}^{c o n d T}\right)^{2} \tag{3}
\end{gather*}
$$

$$
\begin{equation*}
P_{c o n d D}=v_{D 0} \cdot I_{a v g}^{c o n d D}+r_{d D} \cdot\left(I_{r m s}^{c o n d D}\right)^{2} \tag{4}
\end{equation*}
$$

where: $v_{C E 0}, r_{d T}, v_{D 0}$ and $r_{d D}$ - parameters of the transistors and diodes, $I_{\text {avg }}^{\text {cond } X}$ and $I_{r m s}^{c o n d X}$ - average and RMS values of the conduction current through $X$ semiconductor.
The expressions for conduction losses depend on the RMS load current ( $I$ ). The paper presents an example to calculate the conduction losses in $\mathrm{T}_{1}$ transistor from the $\mathrm{S}_{1}$ switch (3L-SC, 3L-NPC and 3L-ANPC).
The modulation function for $\mathrm{T}_{1}$ is sinusoidal:

$$
\begin{equation*}
f_{T l}(x)=M \cdot \sin x, \quad x \in[0, \pi] \tag{5}
\end{equation*}
$$

The $\mathrm{T}_{1}$ transistor is in conduction during $[\theta, \pi]$ interval. As a result, the average and RMS values of the conduction current through $\mathrm{T}_{1}$ semiconductor can be written:

$$
\begin{align*}
& \quad I_{\text {avg }}^{\operatorname{cond} T 1}=\frac{1}{2 \pi} \int_{\theta}^{\pi} \sqrt{2} \cdot I \cdot \sin (x-\theta) \cdot f_{T 1}(x) \cdot d x=  \tag{6}\\
& =\frac{I \cdot \sqrt{2} \cdot M}{4 \cdot \pi} \cdot[(\pi-\theta) \cdot \cos \theta+\sin \theta] \\
& I_{r m s}^{\operatorname{con} d T 1}=\sqrt{\frac{1}{2 \pi} \int_{\theta}^{\pi}(\sqrt{2} \cdot I \cdot \sin (x-\theta))^{2} \cdot f_{T 1}(x) \cdot d x}=  \tag{7}\\
& =I \cdot \sqrt{\frac{M}{2 \pi} \cdot\left[1+\frac{4}{3} \cdot \cos \theta+\frac{1}{3} \cdot \cos (2 \cdot \theta)\right]}
\end{align*}
$$

For the other switches, the losses are similarly calculated but the modulation functions and the conduction intervals differ from a switch to another for each structure.

## B) Switching losses

The IGBTs designers deliver characteristics for the consumed energy at the turning off $E_{\text {off }}\left(I_{C}\right)$ and the consumed energy at the turning on $E_{o n}\left(I_{C}\right)$. These characteristics depend on the switched voltage $\left(v_{\text {def }}\right)$ and on the switched current. For an entire switching period, the total energy absorbed by a semiconductor device at $v_{d e f}$ corresponds to the sum of these energies:

$$
\begin{equation*}
E_{v d e f}\left(I_{C}\right)=E_{o n}\left(I_{C}\right)+E_{o f f}\left(I_{C}\right) \tag{8}
\end{equation*}
$$

This sum (8) can be approximated with a parabola with $A_{s w X}, B_{s w X}$ and $C_{s w X}$ coefficients:

$$
\begin{equation*}
E_{v d e f}\left(I^{s w X}\right)=A_{s w X}+B_{s w X} \cdot I_{\text {avg }}^{s w X}+C_{s w X} \cdot\left(I_{r m s}^{s w X}\right)^{2} \tag{9}
\end{equation*}
$$

The following proportionality law is used to take into consideration the real commutation voltage ( $v_{s w}$ ) for transistors:

$$
\begin{equation*}
E_{v d e f}\left(v_{s w}, I^{s w X}\right)=\frac{v_{s w}}{v_{d e f}} \cdot E_{v d e f}\left(I^{s w X}\right) \tag{10}
\end{equation*}
$$

For a semiconductor device which switch at $f_{s w}$ on $\Delta_{s w}$ interval the losses in commutation can be written as follows:

$$
\begin{align*}
& P_{s w X}=f_{s w} \cdot \frac{v_{s w}}{v_{d e f}} \cdot\left(A_{s w X} \cdot \Delta_{s w}+B_{s w X} \cdot I_{a v g}^{s w X}+\right.  \tag{11}\\
& \left.+C_{s w X} \cdot\left(I_{r m s}^{s w X}\right)^{2}\right)
\end{align*}
$$

where, $A_{s w X}, B_{s w X}, C_{s w X}$ and $v_{d e f}-$ constants taken from the IGBT's characteristics, $\Delta_{s w}$ - ratio between the switching interval and the switching period for semiconductor device, $I_{a v g}^{s w X}$ and $I_{r m s}^{s w X}$ - average and RMS values of the switched current through $X$ semiconductor, $f_{s w}$ - switching frequency and $v_{s w}-$ switched voltage.
The expressions for switching currents also depend on the commutation intervals and on the RMS load current ( $I$ ). The paper presents an example to calculate the switching losses in $\mathrm{T}_{1}$ transistor from the $\mathrm{S}_{1}$ switch (3L-SC, 3L-NPC and 3L-ANPC). This transistor switches on $[\theta, \pi]$ interval. As a result, the average and RMS values of the switching current through $\mathrm{T}_{1}$ semiconductor can be written as follows:

$$
\begin{align*}
& I_{a v g}^{s w T 1}=\frac{1}{2 \pi} \int_{\theta}^{\pi} \sqrt{2} I \sin (x-\theta) d x=\frac{I \sqrt{2}}{2 \pi}(1+\cos (\theta))( \\
& I_{r m s}^{s w T 1}=\sqrt{\frac{1}{2 \pi} \int_{\theta}^{\pi}(\sqrt{2} I \sin (x-\theta))^{2} \cdot d x}=  \tag{13}\\
&=I \sqrt{\frac{1}{2 \pi} \cdot\left(\pi-\theta+\frac{\sin (2 \theta)}{2}\right)}
\end{align*}
$$

This paper compares the losses in power devices between three popular topologies 3L-SC, 3L-NPC and 3L-ANPC. The commutation cells are composed by IGBT modules type Eupec FF200R33KF2C, and the clamp diodes are equivalent to the IGBT module diodes.

### 3.2. Loss Distribution in Power Devices

The losses in power devices depend on the PWM strategy. In the case of analysed converters, there are commutation cells that switch at a low frequency and others that switch at a high frequency. The last ones were controlled by sinusoidal duty cycles. The PWM strategies used to control the popular 3L structures are equivalent and lead to the same output voltages $v_{A O}$. The critical points are located at the boundaries of the converter's operating area, being maximum and minimum modulation index $(M)$, at power factor of $\mathrm{PF}=1$ and $\mathrm{PF}=-1$. In these points the loss distribution presents the biggest lack of balance. All the other operation points are less critical.
Fig. 4 shows the loss distribution in switches for 3LSC, 3L-NPC and 3L-ANPC structures. They were
considered two extreme values of modulation index ( $M=0.05$ and $M=0.95$ ) and six values for power factor ( $\mathrm{PF}=1 ; 0.86 ; 0.707 ; 0.5 ; 0$ and -1 ). The next were observed:

- the middle stage switches $\left(\mathrm{S}_{1 \mathrm{c}}\right.$ and $\left.\mathrm{S}_{3}\right)$ from 3L-SC topology limit the maximum phase current at low modulation indexes;
- in the case of 3L-NPC operation mode, at higher modulation index, total losses in switches are not very different from 3L-SC structure;
- for high values of modulation index, the devices that limit the switching frequency and the maximum phase current are the outer ones, as follow: for 3L-SC $-\mathrm{S}_{1}$ and $\mathrm{S}_{3 \mathrm{c}}$, for 3L-NPC $-\mathrm{S}_{1}$ and $\mathrm{S}_{2 \mathrm{c}}$ and for 3L ANPC $-\mathrm{S}_{1}$ and $\mathrm{S}_{3 c}$; this leads to the increase of the junction temperature in power devices which limits the converters output power;
- in the case of low modulation index, the losses distribution in switches is more uniform in 3LNPC and 3L-ANPC than in 3L-SC;
- at high modulation index and low power factor/rectifier operation mode the losses distribution in switches is more uniform in 3LANPC than 3L-NPC or 3L-SC.
A better loss-balancing ensures that the operating junction temperatures of all devices do not exceed their limits under all specified operation conditions.


## 4. EPERIMENTAL RESULTS

A prototype was made in order to prove the 3L-SC structure operation. The control side uses a FPGA card (Field-Programmable Gate Array) type EP1K100QC208-1 from ACEX1K family.
The supply voltage $V_{D C}$ was equal to 200 V , the switching frequency $f_{s w}$ was 8 kHz and the dead time was $1 \mu \mathrm{~s}$. A RL load ( $\mathrm{R}=16.7 \Omega$ and $\mathrm{L}=6 \mathrm{mH}$ ) was connected between A and O terminals. A PWM control strategy shown in Fig. 2 was implemented. The cells 1 and 3 switch at a high frequency ( 8 kHz ) and the cell 2 switches at a low frequency $(50 \mathrm{~Hz})$, equal with the output voltage frequency. Fig. 5 shows the voltage between A and O terminals $\left(v_{A O}\right)$, the current through the load ( $i_{\text {load }}$ ) and the control signal for $S_{1}$ switch. It is noticed that $S_{1}$ switches only on a half duty cycle, which reduces to $50 \%$ the average switching frequency.

## 5. CONCLUSIONS

In this paper the states and commutation sequences for three of the most popular 3L topologies (3L-SC, 3LNPC and 3L-ANPC) were analysed. Only two of these topologies (3L-SC and 3L-ANPC) are made of two conversion stages. In the case of 3L-SC structure these stages are not completely decoupled, while in the 3L-

ANPC one the conversion stages are completely decoupled. This advantage confers to the 3L-ANPC topology more degrees of freedom, which can be used to develop some PWM control strategies with high performances. PWM sinusoidal strategies were used to
control the structures in order to obtain the same output voltages.
It is also presented an analytic method to calculate the total losses in power devices and it is investigated the loss distribution among the semiconductor devices.


Fig.4. Simulated loss distribution in popular 3L topologies (Eupec FF200R33KF2C IGBTs, $I=130 \mathrm{~A}$, $V_{D C}=3000 \mathrm{~V}, f_{s w}=1000 \mathrm{~Hz}$ ): (a) $3 \mathrm{~L}-\mathrm{SC}(M=0.05)$, (b) $3 \mathrm{~L}-\mathrm{SC}(M=0.95)$, (c) $3 \mathrm{~L}-\mathrm{NPC}(M=0.05)$, (d) $3 \mathrm{~L}-\mathrm{NPC}$ ( $M=0.95$ ), (e) 3L-ANPC ( $M=0.05$ ), (f) 3L-ANPC ( $M=0.95$ ).


Fig.5. Experimental results for the 3L-SC structure: $\mathrm{V}_{\mathrm{AO}}$ output voltage ( $100 \mathrm{~V} / \mathrm{div}$ ), load current ( $5 \mathrm{~A} /$ div) and $\mathrm{S}_{1}$ control ( $\mathrm{M}=0.9 ; 5 \mathrm{~ms} / \mathrm{div}$ ).

This analysis shows that the total losses in studied converters are not different, but the loss distribution in switches is unequal and it depends on the type of
structure, the modulation index and the power factor. The losses in the most stressed switches limit the operation frequency and the maximum phase current
of the entire converter. Between the studied structures, the 3L-ANPC topology allows a better loss balancing in switches, both at low and high values of modulation index, for any power factor.

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