

TOTAL LOSS DISTRIBUTION IN THREE-LEVEL STACKED NPC CONVERTER

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Abstract 4 Static converters design has to ensure that in all specific operating conditions the junction temperature of power devices does not exceed the admitted limits. The junction temperature of power devices is a direct consequence of conduction and switching losses. The unequal distribution of losses among the semiconductors represents one major disadvantage for 3L-SC (Stacked Cells) and 3L-NPC (Neutral Point Clamped) converters. The paper studies the loss distribution problem for 3L-SC and 3L-NPC topologies and proposes the 3L-SNPC (Stacked NPC) converter to overcome this drawback. A numeric calculus method for the total losses in switches was developed in order to compare the analyzed structures. The 3L-SNPC converter allows the natural doubling of the apparent switching frequency and leads to a better balancing of total losses.

Keywords: Three-level converters, Power losses, Voltage source converter.

1. INTRODUCTION

Multilevel structures have been studied for over 25 years and they represent an intelligent solution to connect serial switches [1]. The first developed topology consisted in a serial connection of single-phase inverters with DC separate sources [2]. This structure was followed by a stacked commutation cells concept in order to obtain a multilevel conversion (SC – Stacked Cells) [3-4]. Following the SC structure, a new multilevel NPC (Neutral Point Clamped) topology was developed [5]. This is the most popular multilevel conversion structure. The 3L-NPC converter are considered a particular way of implementing the 3L-SC topology. The role of the middle switches in the 3L-SC structure is taken by the inner switches and by the 2 clamp diodes. Later, another invention [6] introduced the concept of the multilevel converter with flying-capacitors (FC – Flying Capacitor). In the range of low and moderate switching frequencies (200Hz – 1kHz), the 3L-NPC converter is especially advantageous because of the required flying-capacitor size, which is inversely proportional to the switching frequency. The 3L-NPC structure performances were improved by developing the 3L-ANPC (Active NPC) converter [7-8].

Recently, a new structure 3L-SNPC (Stacked NPC) was developed [9-10]. This converter is a combination between 2 well-known 3L concepts (3L-SC and 3L-NPC) and it improves the static conversion.

This paper calculates and compares the losses in power devices between three 3L topologies: 3L-SC, 3L-NPC and 3L-SNPC. The structures are composed by IGBT modules type Eupec FF200R33KF2C, and the clamp diodes are equivalent to the IGBT modules' diodes. The switching states and commutations of the converters are analyzed and their influence on the balancing of losses within the converter is explained.

A numeric calculus method for total losses in switches was elaborated to compare the studied structures. The analytic expressions for medium and effective currents in conduction and switching states were also calculated. A validation of these expressions was made using PSIM simulations. The analysis made on the 3L-SC and 3L-NPC topologies proved that the losses in middle side power devices (3L-SC) and the losses in inner switches (3L-NPC) increase simultaneously with the reducing of the modulation index. This leads to the increase of the junction temperature in power devices, which limits the converters output power and the switching frequency, especially at zero speed operating. The paper shows that 3L-SNPC structure has more degrees of freedom and allows a better balancing of losses in power devices.

2. POPULAR THREE-LEVEL STRUCTURES

2.1. Three-Level SC Converter

The 3L-SC structure is made of 6 switches disposed on three sides (Fig.1). Each switch is capable to support a voltage equal to $V_{DC}/2$. The exterior sides are made of 2 switches serially connected and the middle side is composed by 2 switches opposite connected. The switches form 3 commutation cells controlled with ζ_1 , ζ_2 and ζ_3 duty cycles: cell 1 (S_1 - S_{1c}), cell 2 (S_2 - S_{2c}) and cell 3 (S_3 - S_{3c}). A sinusoidal PWM strategy was used in order to emphasize the constraints applied to 3L-SC converter [9].

The PWM strategy has 4 switching states (Table 1). Two switching states (P and N) correspond to direct connection of the load at DC voltage and the other two correspond to obtain zero states (O_1^- and O_2^+). For the state P ($V_{DC}/2$) the switches S_1 , S_2 and S_3 must be turned on. For the state N ($-V_{DC}/2$) the switches S_{1c} , S_{2c} and S_{3c} must be turned on.

The state O_1^- is obtained when the reference output voltage is negative. In this case, the S_{1c} , S_{2c} and S_3 are turned on. The state O_2^+ is obtained when the reference output voltage is positive. For this switching sequence the S_{1c} , S_2 and S_3 must be turned on.

A calculus methodology for the total losses in switches was developed in order to emphasize the unequal distribution of losses. This methodology was first carried out in [11], and was extended in section 4. By using this methodology for the analyzed 3L structures, it has been observed that the conduction and switching losses of the power devices depend on the operating points and on the PWM strategy. The most critical operating points are located at the boundaries of the converter's operating area, being maximum and minimum modulation depth (M), at power factor PF=1 and PF=-1.

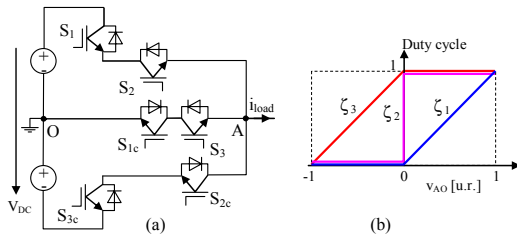


Figure 1: Three-level SC converter: (a) topology, (b) duty cycle control.

Output Voltage (v_{AO})	Switching State	Switch Sequence					
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}
$-V_{DC}/2$	N	0	1	0	1	0	1
0	O^-	0	1	0	1	1	0
	O^+	0	1	1	0	1	0
$V_{DC}/2$	P	1	0	1	0	1	0

Table 1: Switching sequences of 3L-SC converter.

Fig.2 shows the conduction (P_{con}) and switching losses (P_{sw}) for 2 operating modes. The losses for the switches were emphasized when the distribution is most unbalanced. All operating points in between are less critical.

In the case of PF=-1 and small modulation index (M=0.05) the middle side transistors (T_{1c} and T_3) are the most stressed devices for rectifier operating mode [Fig.2(a)]. The transistors from exterior sides (T_1 and T_{3c}) are the most stressed devices for inverter operating mode, when PF=1 and M=0.95 [Fig.2(b)].

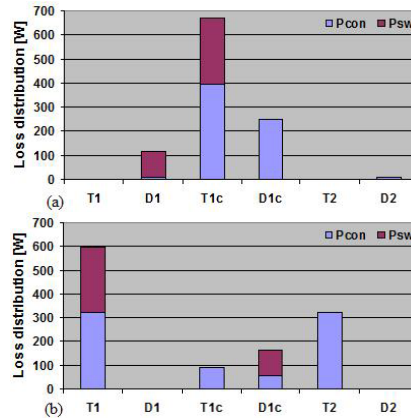


Figure 2: Simulated distribution of losses in 3L-SC converter featuring Eupec IGBTs ($V_{DC}=3000V$, $I_{rms}=200A$, $f_s=1000Hz$, Eupec FF200R33KF2C): (a) PF=-1, M=0.05, (b) PF=1, M=0.95.

2.2. Three-Level SC Converter

The 3L-NPC is the most popular 3L topology [Fig.3(a)]. It is composed by 4 bidirectional switches and 2 clamp diodes. Each switch is capable to support a voltage equal to $V_{DC}/2$. The switches form 2 basic commutation cells: cell-1 (S_1-S_{1c}) and cell-2 (S_2-S_{2c}). These are controlled by ζ_1 and ζ_2 duty cycles. The duty cycle presented in Fig.3(b) was used to analyze the switching states.

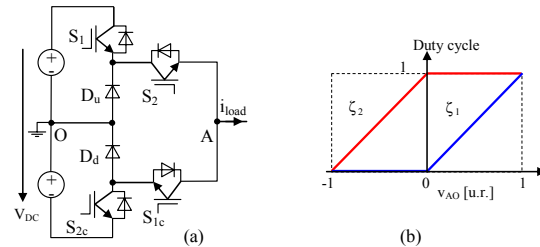


Figure 3: Three-level NPC converter: (a) topology, (b) duty cycle control.

The 3L-NPC topology has only 3 switching states: P, O and N (Table 2). The P and N states correspond to a direct connecting of the load with the DC supply voltage. The P state is obtained by turning on the switches S_1 and S_2 . Similarly, the N state is obtained by turning on the S_{1c} and S_{2c} .

Output Voltage (v_{AO})	Switching State	Switch Sequence			
		S_1	S_{1c}	S_2	S_{2c}
$-V_{DC}/2$	N	0	1	0	1
0	O	0	1	1	0
$V_{DC}/2$	P	1	0	1	0

Table 2: Switching sequences of 3L-NPC converter.

The zero state is obtained when the inner switches S_{1c} and S_2 are turned on. In this case, the inductive load current passes through 2 different paths, depending on its direction. If the load current is positive, the paths will be through the D_u diode and S_2 . If the load current is negative, the paths will be through D_d and S_{1c} . The existence of a single one switching zero state represents a limitation on the 3L-NPC structure that has direct consequences for the distribution of losses among the switches.

Fig.4 shows the conduction and switching losses (P_{con} and P_{sw}) for 2 operating modes. They were emphasized the losses for the outer and inner switches and for the clamp diodes when the distribution is most unbalanced. All operating points in between are less critical. In the case of $PF=-1$ and small modulation index ($M=0.05$) the inner transistors (T_2 and T_{1c}) are the most stressed devices for rectifier operating mode [Fig.4(a)]. The outer transistors (T_1 and T_{2c}) are the most stressed devices for inverter operating mode, when $PF=1$ and $M=0.95$ [Fig.4(b)].

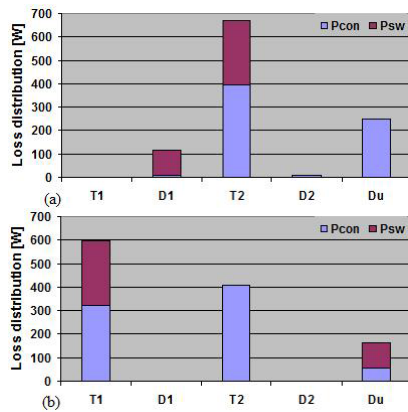


Figure 4: Simulated distribution of losses in 3L-NPC converter featuring Eupec IGBTs ($V_{DC}=3000V$, $I_{rms}=200A$, $f_s=1000Hz$, Eupec FF200R33KF2C): (a) $PF=-1$, $M=0.05$, (b) $PF=1$, $M=0.95$.

3. THREE-LEVEL SNPC CONVERTER

The 3L-SNPC (Stacked Neutral Point Clamped) converter represents a static conversion concept with three voltage levels [Fig.5(a)].

The 3L-SNPC converter is composed by 6 bidirectional switches disposed on 3 sides and 2 clamp diodes [9-10]. The exterior sides are made of 2 switches serially connected (S_1 - S_2 and S_{2c} - S_{3c}) and the middle side is composed by 2 switches oppositely connected (S_{1c} - S_3). Each switch is capable to support a voltage equal to $V_{DC}/2$. The bidirectional switches are grouped in 3 basic commutation cells: cell-1 (S_1 - S_{1c}), cell-2 (S_2 - S_{2c}) and cell-3 (S_3 - S_{3c}). These are controlled by ζ_1 , ζ_2 and ζ_3 duty cycles [Fig.5(b)].

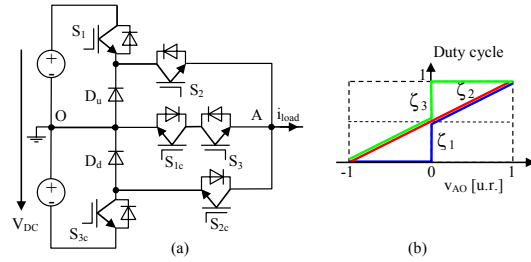


Figure 5: Three-level SNPC converter: (a) topology, (b) duty cycle control.

The clamp diodes D_u and D_d are similarly connected to the 3L-NPC converter. The 3L-SNPC converter has more degrees of freedom and can be controlled with different PWM strategies. In this paper a sinusoidal PWM strategy is presented (Fig.6). It allows the natural doubling of the apparent switching frequency. The intention is not to save total converter losses, but to distribute them equally. In order to emphasize this advantage, the states and sequences are analyzed at one switching period T_s .

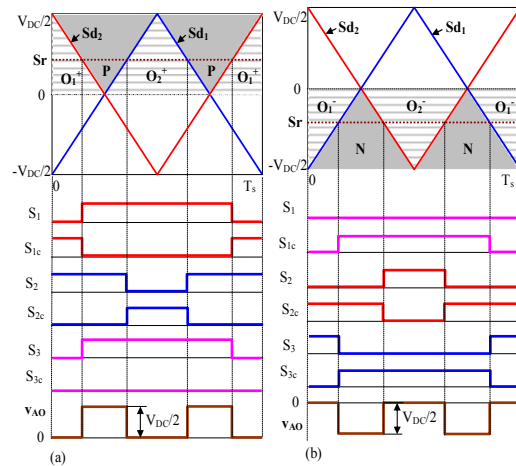


Figure 6: Sinusoidal PWM for 3L-SNPC converter: (a) $Sr > 0$, (b) $Sr < 0$.

The reference voltage Sr is compared with 2 carrier waves S_{d1} and S_{d2} that are phase-shifted on the horizontal axis with $T_s/2$. The 3L-SNPC has 6 switching states: P, N, O_1^- , O_2^- , O_1^+ and O_2^+ (Table 3). The switches S_1 , S_2 and S_3 must be turned on in order to obtain the switching state P ($V_{DC}/2$). The state N ($-V_{DC}/2$) is obtained by turning on the switches S_{1c} , S_{2c} and S_{3c} . In the case of P and N sequences the load current paths through the switches are the same with the other 3L converters studied in the paper. For the zero states, 4 different control sequences are used: O_1^- , O_2^- , O_1^+ and O_2^+ . The state O_1^- is obtained when the switches S_{2c} and S_3 are turned on and S_1 , S_{1c} , S_2 and S_{3c} are turned off.

Output Voltage (v_{AO})	Switching State	Switch Sequence					
		S_1	S_{1c}	S_2	S_{2c}	S_3	S_{3c}
$-V_{DC}/2$	N	0	1	0	1	0	1
0	O_1^-	0	0	0	1	1	0
	O_2^-	0	1	1	0	0	1
	O_1^+	0	1	1	0	0	0
	O_2^+	1	0	0	1	1	0
$V_{DC}/2$	P	1	0	1	0	1	0

Table 3: Switching sequences of 3L-SNPC converter.

If the load current is positive, it will pass through the switches from the middle side (S_{1c} and S_3). If the load current is negative, it will pass through S_{2c} and the clamp diode D_d . The state O_2^- is obtained when S_{1c} , S_2 and S_{3c} are turned on and S_1 , S_{2c} and S_3 are turned off. Depending on its direction, the inductive load current will pass through 2 different paths. If the load current is positive, it will pass through S_2 and clamp diode D_u . If the load current is negative the path will be through the switches contained in the middle side (S_{1c} and S_3). The state O_1^+ is obtained when the switches S_{1c} and S_2 are turned on and S_1 , S_{2c} , S_3 and S_{3c} are turned off. The paths of the load current are similarly with the state O_2^- . The state O_2^+ is obtained when S_1 , S_{2c} and S_3 are turned on and the switches S_{1c} , S_2 and S_{3c} are turned off. The paths of the load current are similarly with the O_1^- case.

These switching sequences lead to a natural doubling of the apparent switching frequency similar to the flying-capacitor concept (3L-FC), although the 3L-SNPC converter does not have flying-capacitors.

Another advantage of the PWM strategy consists in the natural improving of the static conversion when the reference voltage is close to zero value. The dead times do not influence the operating of the converter at $S_r \approx 0$, because the commutations are made by using 2 different basic cells. Thus, close to zero voltage, when $S_r > 0$ the cells 1 and 2 switch and when $S_r < 0$ the cells 2 and 3 switch. The control principle can be used at every switching frequency (higher or lower) without requiring structural changes in the frame of the structure (e.g. modification of some flying capacitors, as in the case of 3L-FC converter).

Fig.7 shows the conduction and switching losses (P_{con} and P_{sw}) for both operating modes (rectifier/inverter) in the most critical operating points. All operating points in between are less critical.

In the case of $PF=-1$ and small modulation index ($M=0.05$) the switches T_{1c} , T_2 , T_3 and T_{2c} are the most stressed devices in rectifier operating mode [Fig.7(a)]. It is observed that in comparison with 3L-NPC and 3L-SC structures the 3L-SNPC allows a decrease of 50% of the total losses in the most stressed switches. The inner transistors (T_2 and T_{2c}) are the most stressed devices in inverter operating

mode when $PF=1$ and $M=0.95$ [Fig.7(b)]. In this case, the total losses in the most stressed switches are reduced with 20% in comparison with the other studied structures, without any additional semiconductor expense.

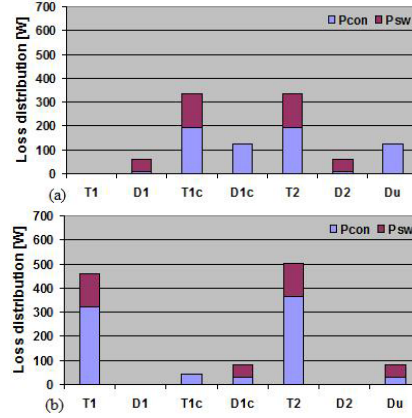


Figure 7: Simulated distribution of losses in 3L-SNPC converter featuring Euepc IGBTs ($V_{DC}=3000V$, $I_{rms}=200A$, $f_s=1000Hz$, Euepc FF200R33KF2C): (a) $PF=-1$, $M=0.05$, (b) $PF=1$, $M=0.95$.

4. CALCULUS OF TOTAL LOSSES

The evolution of temperature in IGBT modules is a direct consequence of the total losses and imposes the maximum power that can be delivered by power switches.

The following hypotheses were considered to calculate the losses in power devices:

- € the load current is sinusoidal;
- € the current and voltage ripples are neglected;
- € the dead times of the IGBT modules are neglected.

The total losses (P_X) are made of conduction losses and switching losses:

$$P_X = P_{conX} + 2 P_{swX} \quad (1)$$

4.1. Conduction losses

The conduction losses are obtained as a sum of conduction losses in transistors (P_{conT}) and diodes (P_{conD}):

$$P_{conX} = P_{conT} + 2 P_{conD} \quad (2)$$

$$P_{conT} = v_{CE0} \int_{avg}^{conT} 2 r_{dT} \int_{rms}^{conT} \vartheta \quad (3)$$

$$P_{conD} = v_{D0} \int_{avg}^{conD} 2 r_{dD} \int_{rms}^{conD} \vartheta \quad (4)$$

where: v_{CE0} , r_{dT} , v_{D0} and r_{dD} – parameters of the transistors and diodes, I_{avg}^{conX} and I_{rms}^{conX} – average and RMS values of the conduction current through X semiconductor.

The expressions for conduction losses depend on the RMS load current (I). The paper presents an example to calculate the conduction losses in T_1 transistor from the S_1 switch (3L-SC, 3L-NPC and 3L-SNPC).

The modulation function for T_1 is sinusoidal:

$$f_{T1}/x0 | M \sin x, \quad x \in \Psi, \phi \beta \quad (5)$$

The T_1 transistor is in conduction during $[\chi, \phi]$ interval. As a result, the average and RMS values of the conduction current through T_1 semiconductor can be written:

$$I_{avg}^{conT1} | \frac{1}{2\phi} \int_{\chi}^{\phi} \sqrt{2} I \sin/x 4 \chi 0 (f_{T1}/x0) dx | \quad (6)$$

$$| \frac{I \sqrt{2} M}{4 \phi} \int_{\chi}^{\phi} 4 \chi 0 \cos \chi 2 \sin \chi \beta$$

$$I_{rms}^{conT1} | \sqrt{\frac{1}{2\phi} \int_{\chi}^{\phi} \sqrt{2} I \sin/x 4 \chi 0^2 (f_{T1}/x0) dx |} \quad (7)$$

$$| I \sqrt{\frac{M}{2\phi} \left(12 \frac{4}{3} \cos \chi 2 \frac{1}{3} \cos/2 \chi 0 \right)}$$

For the other switches, the conduction losses are similarly calculated but the modulation functions and the conduction intervals differ from a switch to another for each structure.

4.2. Switching losses

The IGBTs designers deliver the characteristics for the consumed energy at the turning off $E_{off}(I_C)$ and the consumed energy at the turning on $E_{on}(I_C)$. These characteristics depend on the switched voltage (v_{def}) and on the switched current I_C . For an entire switching period, the total energy absorbed by a semiconductor device at v_{def} corresponds to the sum of these energies:

$$E_{v_{def}/I_C 0} | E_{on}/I_C 0 2 E_{off}/I_C 0 \quad (8)$$

This sum (8) can be approximated with a parabola with A_{swX} , B_{swX} and C_{swX} coefficients:

$$E_{v_{def}/I_C 0} | A_{swX} 2 B_{swX} \int_{avg}^{swX} 2 C_{swX} \int_{rms}^{swX} \quad (9)$$

The following law of proportionality is used to take into account the real commutation voltage (v_{sw}) for transistors:

$$E_{v_{def}/v_{sw}, I_C^{swX}} | \frac{v_{sw}}{v_{def}} (E_{v_{def}/I_C^{swX}}) \quad (10)$$

For a semiconductor device that switches at f_s on τ_{sw} interval, the switching losses can be written as follows:

$$P_{swX} | f_s \frac{v_{sw}}{v_{def}} \left(A_{swX} \tau_{sw} 2 B_{swX} I_{avg}^{swX} 2 C_{swX} I_{rms}^{swX} \right) \quad (11)$$

where, A_{swX} , B_{swX} , C_{swX} and v_{def} – constants taken from the IGBT's characteristics; Δ_{sw} – ratio between the switching interval and the switching period for semiconductor device; I_{avg}^{swX} and I_{rms}^{swX} – average and RMS values of the switched current through X semiconductor, f_s – switching frequency and v_{sw} – switched voltage.

The expressions for switching currents also depend on the commutation intervals and on the RMS load current (I). The paper presents an example to calculate the switching losses in T_1 transistor from the S_1 switch (3L-SC, 3L-NPC and 3L-SNPC). This transistor switches on $[\chi, \phi]$ interval. As a result, the average and RMS values of the switching current through T_1 semiconductor can be written as follows:

$$I_{avg}^{swT1} | \frac{1}{2\phi} \int_{\chi}^{\phi} \sqrt{2} I \sin/x 4 \chi 0 dx | \quad (12)$$

$$| \frac{I \sqrt{2}}{2\phi} \int_{\chi}^{\phi} 2 \cos/x 0$$

$$I_{rms}^{swT1} | \sqrt{\frac{1}{2\phi} \int_{\chi}^{\phi} \sqrt{2} I \sin/x 4 \chi 0^2 dx |} \quad (13)$$

$$| I \sqrt{\frac{1}{2\phi} \left(\int_{\chi}^{\phi} 4 \chi 2 \frac{\sin/2 \chi 0}{2} \right)}$$

For the other switches, the switching losses are similarly calculated but the commutation intervals differ from a switch to another for each structure.

5. CONCLUSIONS

In this paper the distribution of losses among the semiconductors in the three-level SC and NPC converters has been investigated. The analysis shows an unequal distribution, which severely limits the output power of the converter. The 3L-SC and 3L-NPC concepts were extended to the 3L-SNPC concept, in order to overcome this drawback. A numeric calculus method for total losses in switches was elaborated to compare the studied structures and the analytic expressions for average and effective currents in conduction and switching states were also calculated. A validation of these expressions has been made using PSIM simulations.

The 3L-SNPC converter has more degrees of freedom and can be controlled with different PWM strategies. The sinusoidal PWM strategy described in the paper presents new switching states and commutations that enable a substantial improvement of the unequal distribution. The performances of this PWM strategy have been compared with other 3L structures. The total losses in 3L-SNPC converter are not smaller, but a better balancing of losses is obtained. The 3L-SNPC topology allows the natural

doubling of the apparent switching frequency, similarly with the 3L-FC concept. This represents an important advantage because the 3L-SNPC converter does not have flying-capacitors.

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