A Low Power Discreet Time Sigma Delta Modulator in 50nm CMOS Digital

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Abstract—Sigma delta modulators (ΣΔMs) form part of the core of today's mixed-signal designs. The ongoing research on these devices shows the potential of ΣΔ data converters as a promising candidate for high-speed, high-resolution, and low power mixed-signal interfaces. This paper presents a new circuit realization for discreet time sigma delta modulator. The modulator is designed in 50nm CMOS digital technology and features low power consumption (<100uW), low supply voltage (±1.2), and wide dynamic range (>70db). The performance of the circuits was demonstrated using HSPICE at low voltage operation of ±1.2V. The modulator was used to design 11bit second order ΣΔ ADC. This architecture is an attractive approach to implementing precision A/D convertors in scaled digital VLSI technologies.