ADVANCES ON PARASITIC CAPACITANCE REDUCTION OF EMI FILTERS

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Abstract **– The improvements of EMI integrated filter characteristics suppose two major directions: the first is to increase the HF attenuation (through losses increasing) and the second is the parasite effects suppression of the constituent devices. In this light, the main goal of the paper is to develop and analyse the effectiveness of several EPC-reducing techniques; the present study propose a new method of parasite capacitance reduction that is the staggered winding technique. The effectiveness of these techniques was evaluated by Finite Elements (FEM) simulations. Final conclusions will end the paper.**

Keywords: *EMI filter, parasite capacitance, staggered winding technique.*

1. INTRODUCTION

The parasite capacitance of filter inductor is normally the main parasitic parameter, which hurts the high frequency performance of the EMI filter. Hence it is always desirable to minimize parasite capacitance. As shown in the well-known parallel plate capacitance calculation equation $C= \varepsilon_0\varepsilon_r A/d$, capacitance can be reduced by varying the three parameters: reducing plate area A; increasing distance between plates d and reducing relative permittivity ε_r of the dielectric material.

From the practical point of view, the reduction of the conductive pathways surfaces is not feasible because it could have an important effect on the practical current capability of filter, thus will be considered only the versions which suppose the distance increasing and the reduction of dielectric permittivity between the conductive pathways. Additionally, a new technique is proposed that will be analyzed in details in this study. It is the appliance of a geometrically staggered between windings. These principles considered and applied in case of structural parasite capacitance reduction of the EMI integrated filters.

To evaluate the effectiveness of the EPC-reducing techniques, the parasite capacitances of the four single winding structures shown in Fig.1-5 are computed using a commercial FEM software package.

2. ORIGINAL STRUCTURE

The structure shown in Fig.1 is the original structure,

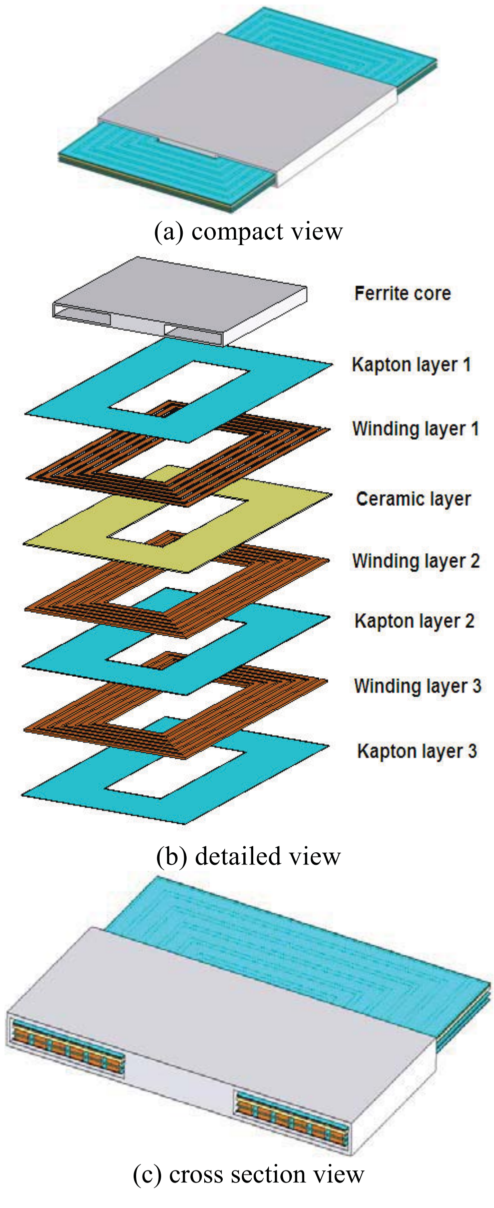
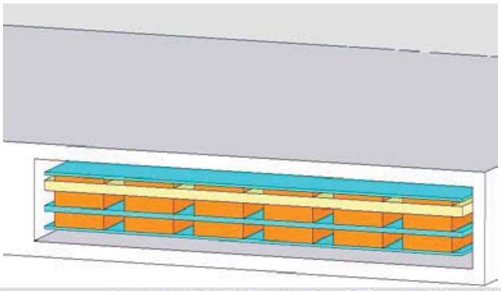


Figure 1: Physical structure of the studied integrated EMI filter

Materials	Ferrite	Air	Cu	Kapton	Ceramic
ε_r	12	1	1	3.6	84

Table 1: Material properties used in the simulation

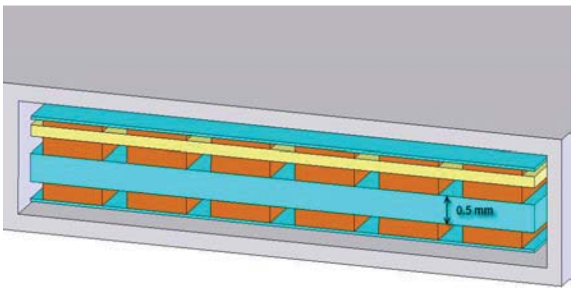
which has two winding layers and six turns per layer. The first winding layer is an integrated L-C winding, consisting of a thin copper winding, a ceramic layer and a thick copper winding. The second winding layer is a normal copper-foil winding. All the conductors have the same dimensions, which are 1.2 x 0.3 mm. The thickness of the insulation kapton between winding layers is 0.1 mm.
The relative permittivity of the materials used in the simulation is given in Table 1.



	winding1	winding2	winding3
winding1	3465.9	-3424.6	-29.768
winding2	-3424.6	3678	-265.28
winding3	-29.768	-265.28	$\boxed{298.38}$

Figure 2: Detailed cross section view and the parasite capacitance calculated for the original structure (i).

3. INCREASED INSULATION THICKNESS



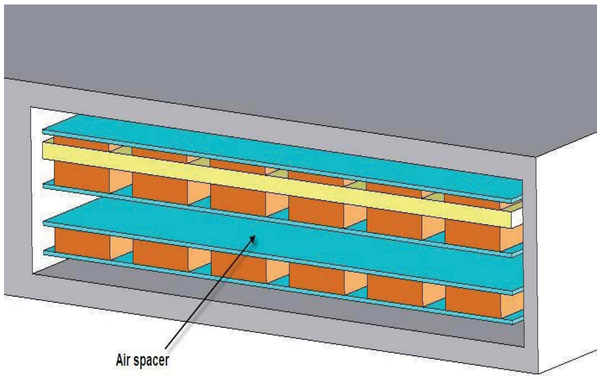
	winding1	winding2	winding3
winding1	3389.6	-3436.5	0
winding2	-3436.5	3490.4	-40.375
winding3	0	-40.375	$\boxed{69.529}$

Figure 3: Detailed cross section view and the effect of increasing the insulation thickness on the parasite capacitance values (ii)

Increasing the distance between plates can be achieved by increasing insulation layer thickness. The structure shown in Fig. 3 is similar to that of Fig. 2, except the insulation kapton thickness is increased to 0.5 mm.

4. AIR SPACER – REDUCING RELATIVE PERMITTIVITY OF INSULATION MATERIAL

Reducing ε_r can be achieved by inserting an "air spacer" between winding layers instead of using the normal insulation material since the relative permittivity of air is approximately 1, while the relative permittivity of other widely-used insulation materials is in the range from 4 to 10. However, there is no solid "air spacer" at room temperature; winding with "air spacer" is not a mechanically stable structure and it is not feasible. Therefore the staggered winding structure shown in Fig. 5 is proposed. The conductors and the thin insulation materials on their surfaces provide the mechanical support to form the "virtual air spacer".
The structure shown in Fig. 4 replaces kapton in Fig. 3 with air.



	winding1	winding2	winding3
winding1	3404.9	-3432.5	-5.9227
winding2	-3432.5	3459	-7.0668
winding3	-5.9227	-7.0668	$\boxed{27.836}$

Figure 4: Detailed cross section view and the effect of the "air spacer" on the parasite capacitance values (iii).

5. STAGGERED WINDING

The cross section view of the proposed staggered winding (iv) is presented in Fig. 5. To avoid the overlapped windings, the number of winding layers is increased to four and the number of windings on each layer is reduced to three.

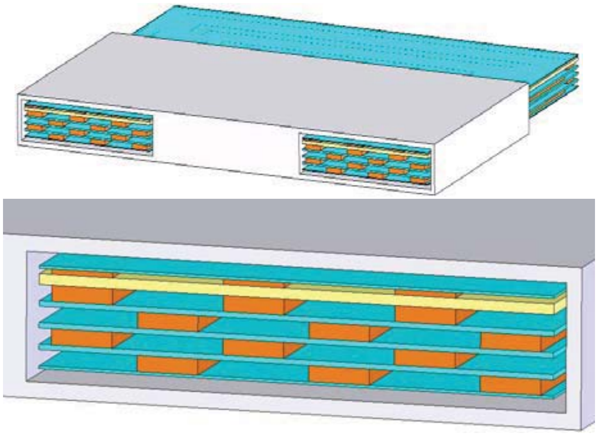
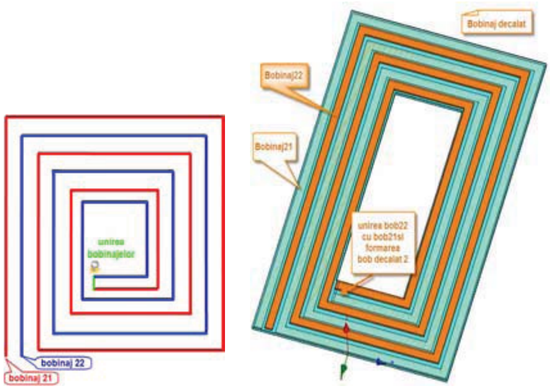
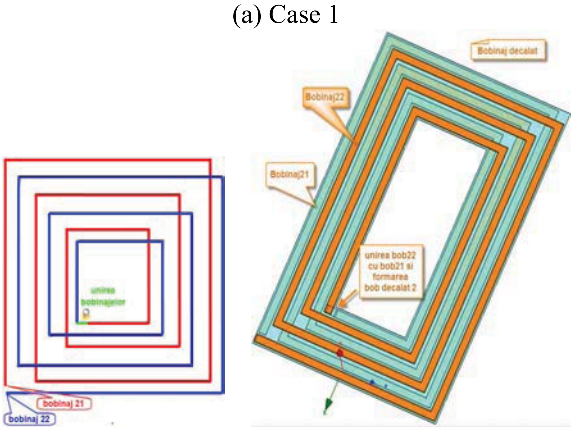


Figure 5: The staggered winding structure.

Two cases were tested for 3D analyze of the staggered winding structure method based on how the staggered winding was realized, see Fig. 6.



(a) Case 1



(b) Case 2

Figure 6: The staggered winding achievement.

In the first case the two cooper layers that form the staggered winding starts both from the same side, and the second case the second *the winding 22* starts from the point where *the winding 21* ends. The staggered winding is obtained connecting both windings.
The two correspondent models of the proposed methods for the staggered winding method are presented in Fig. 7 for Case1 and Fig. 8 for Case 2. As it was mentioned above the only difference between cases is how the staging is realized, the other boards are the same.

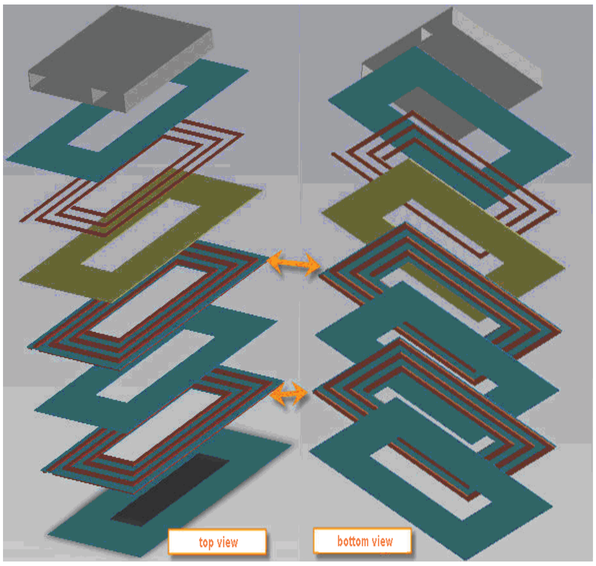


Figure 7: 3D view of staggered winding usage Case 1.

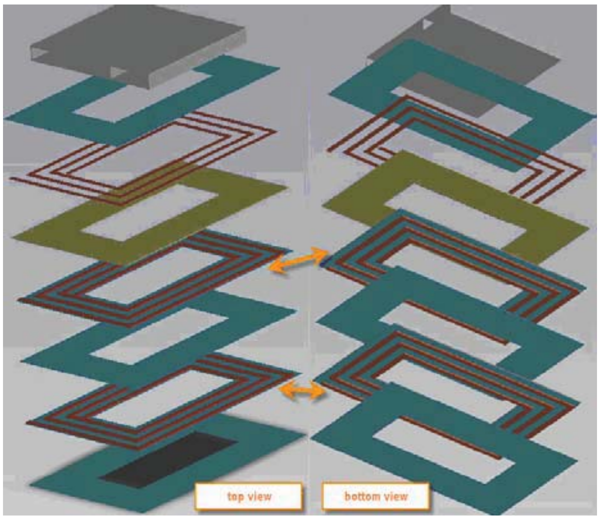
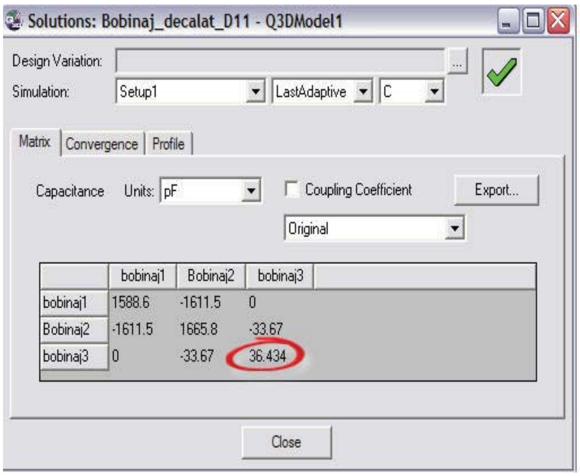


Figure 8: 3D view of staggered winding usage Case 2.

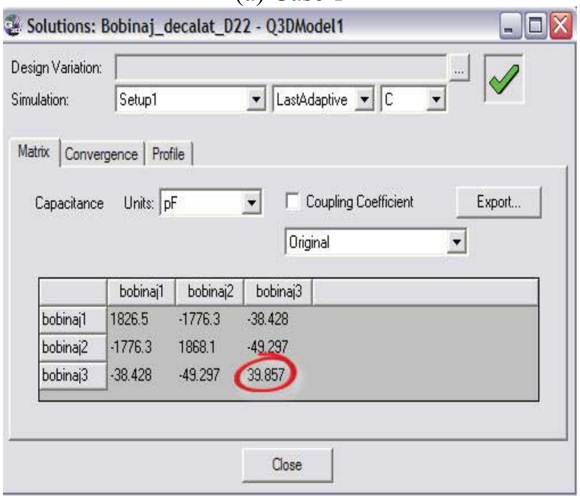
After both cases simulations, the obtained capacitance matrices are presented in Fig. 9.
It is visible that for C_{33} small differences are obtained comparing these matrices.
The C_{33} values for all four simulated structures are gathered in Table 2.

Structure	(i)	(ii)	(iii)	(iv_1)	(iv_2)
ε_r	298	69	27	36	39

Table 2: C_{33} for all four structures.



(a) Case 1



(b) Case 2

Figure 9: Parasite capacitance results – Using the staggered winding structure

Following the numerical modeling results it's visible that using the method of increasing the insulation thickness cause a four times reductions of the parasite capacitance. The kapton 2 layer replacements with an "air spacer" reduce the parasite capacitance with about 11 times related to standard structure, original structure.

The conclusion of complete analyze to reduce the parasite capacitance is that the "air spacer" method is the most effective. Applying this method, the parasite capacitance is a lot reduced, that means an efficient method but, unfortunately from the mechanical point of view it's an unstable structure and it's practically difficult to be realized.

Therefore, the staggered winding method is proposed for parasite capacitance reduction.

4. CONCLUSIONS

The paper outlines several techniques for minimizing the parasite capacitance for EMI filters integration, such as: increased insulation thickness, "air spacer" and staggered winding. Following these techniques, as it was outlined in the paper, the parasite capacitance can be reduced several times with respect to the original traditional arrangement of the winding structure.

Thus, the high frequency performances of an integrated EMI filter could be significantly improved by applying the proposed EPC reduction techniques.

References

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