DESIGN AND PERFORMANCES OF COUPLING PASSIVE FILTERS IN THREE-PHASE SHUNT ACTIVE POWER FILTERS

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***Abstract* – The passive interface filter represents the link between the power grid and the shunt active filter. The interface filter is used both to obtain a good dynamic of the compensating current and to limit the high frequency harmonics due to the power semiconductor devices switching. To obtain an efficient rejection of these harmonics while passing the necesary compensating harmonics, the interface filter must achieve two contradictory conditions, that is, to have a low inductance and a steep frequncy response over the highest harmonic frequency. The second order filters meet these goals, but with the price of instabilty. This paper aims to find an optimal compromise between interface filter stability and the limitation of the power dissipated by the used damping resistors, while achieving maximum performance of the active filtering. A secondary role assigned to the damping resistors is to avoid the operation of the LCL interface filter as a passive harmonics filter connected to the power grid, an undesirable effect which can occur under certain conditions. By proper design of the interface filter, the active filtering performance can increase by several orders of magnitude, without having to increase the compensating capacitor voltage, in the DC circuit of the active filter.**

***Keywords*:** *active filters, interface filters, harmonics, power quality.*

1. INTRODUCTION

The performances achieved by the active filter are directly dependent on the passive interface filter performance. The simplest interface filter is made of three coils, each connected between one phase of the power grid and the corresponding phase of the active filter [3][10]. The role of these coils is to determine the current supplied by the active filter according to the voltage supplied by the power inverter (the current through one coil is determined by the difference between the potential of the grid phase where the coil is connected and the potential of the corresponding inverter phase). Also, the interface filter has the task of limiting the ripple of the compensating current supplied to the nonlinear load, ripple due to the switching of the inverter semiconductor devices. For the correct operation of the active filter, in the choise of the inductance value it must be taken into account that it must be able to compensate the changes in the current supplied by the active filter during one switching period of the power electronic devices [5]. Thus, the passive interface filter inductance value depends on the level of harmonics to be eliminated from the power grid, the active filter DC-Link voltage, and on the switching frequency.

2. THE SECOND ORDER INTERFACE FILTER

The second order interface filter (T filter, generally used) can provide superior rejection of harmonics caused by the switching operation of the active filter, along with its good dynamic response [12]. As seen in figure 1, the interface filter is composed of two inductors and one capacitor [6].

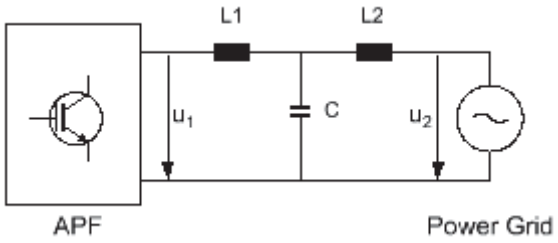

Figure 1: The second order filter schematic diagram

2.1. The filter parameters

For the calculation of the filter parameters, it was started from the filter frequency response, by imposing the bandwidth, being necessary to determine the interface filter transfer function [5].
Considering the power grid voltage being sinusoidal, the passive interface filter will behave like a short circuit to all the current harmonic components, besides the fundamental. It results that the power grid influence on the interface filter transfer function can be neglected.
Following the calculation presented detailed in [5], the interface filter transfer function expression is:

$$H(s)=\frac{I_2(s)}{I_1(s)}=\frac{1}{1+s^2L_2C} \qquad (1)$$

The transfer function is arranged in the standard form of a second order system which makes evident the

resonance natural frequency ω_n and the damping ratio ξ [5]:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2)$$

where:

$$\xi = 0\ ,\ \omega_n = \frac{1}{\sqrt{L_2 C}} \quad (3)$$

In operation, the interface filter must attenuate the high frequency currents due to power electronics switching, and allow the compensating harmonic currents. Therefore, the cutting frequency must be lower than the minimum switching frequency of the inverter if it is controlled by means of hysteresis regulators, but higher than the frequency corresponding to the maximum harmonic order to be compensated by the active filter. Considering the interface filter bandwidth at 3 dB, the relation (3) gives the inequality:

$$\frac{1}{2\pi^2 f_{sw}^2} \le L_2 C \le \frac{1}{8\pi^2 f_{arm}^2} \quad (4)$$

Where f_{sw} is the lowest inverter switching frequency and f_{arm} is the frequency corresponding to the highest harmonic order to be compensated.
Assuming the maximum switching frequency, 10 kHz, and the highest harmonic order to be compensated, 50, (40) gives:

$$0.506 \cdot 10^{-9} \le L_2 C \le 2.02 \cdot 10^{-9} \quad (5)$$

The relation (5) gives a large domain for choosing the values for L_2 and C, therefore, aditional restrictions are necessary for the proper dimensioning of the filter. Of these, the following should be mentioned [5]:

- There is an optimum value of the product L_2C for which the compensated current total harmonic distorsion factor reaches its lowest value;
- The increase of the L_2 inductance over 4 mH imposes the increase of the DC-Link capacitor voltage, in order to ensure the necessary dynamic;
- The interface filter total inductance that minimizes the compensated current total harmonic distorsion factor is about 4 mH.

For a inductance value of 4 mH, the capacity should be between 0.12 and 0.5 μF. The conducted studies, using Matlab Simulink, reveals that the sum of the two inductances must not exceed 5 mH in order to maintain a sufficient dynamic for the active filter. Thus, the inductance L_1 must not exceed 1 mH. For the experimental active filter, L_1 was chosen as 10% of the value of L_2, the total inductance of 4.4 mH resulting less than the maximum value obtained by simulation.

3. THE DAMPING CIRCUIT. TYPES OF DAMPING CIRCUITS

Experimental studies have shown that the resulted LCL filter structure is not sufficiently stable, generating oscillations between the reactive elements of the circuit. Also, due to the very low value of the inductance L_1, the maximum switching frequency for the hysteresis control can reach dangerously high levels.
Another undesirable effect is given by the operation of the interface filter as a passive harmonic filter, therefore, even if the inverter transistors are in off condition, as long as the active filter is connected to the power grid, the interface filter will absorb harmonic currents from the grid, overloading itself, regardless if the active filter is in operating condition or not.
To limit the instability of the LCL interface filter, and also, to avoid the operation as a passive harmonic filter, a resistive damping circuit is required.
For the damping resistor tuning, it should be taken into consideration that the impedance of the passive filter at resonance frequency reaches its minimum, approaching zero, and the inductive reactance equals the capacitive reactance. Thus, the damping resistance should be chosen proportional to the inductive or capacitive reactance [12]:

$$k \cdot R_d = X_{L2} = X_C \quad (6)$$

Three connection options can be used, by mounting the damping resistor towards one of the grid side reactive elements of the passive filter, as follows:

- by mounting the resistor in parallel with the L_1 or L_2 inductance;

- by mounting the resistor in series with the capacitor.

3.1. The parallel connection of the damping resistor

The connection of the resistor in parallel with L_1 is not justified, because this type of connection leads to an increased switching frequency by shunting the inductor used for the hysteresis control. At the same time, this configuration is not preventing the L_2C section of the interface filter to operate as a passive harmonics filter connected to the power grid. By connecting the resistor in parallel with the inductor L_2, the first will be proportional with the inductive reactance of the latter, which, at the resonance frequency of the circuit of 7.95 kHz, amounts to 200Ω.

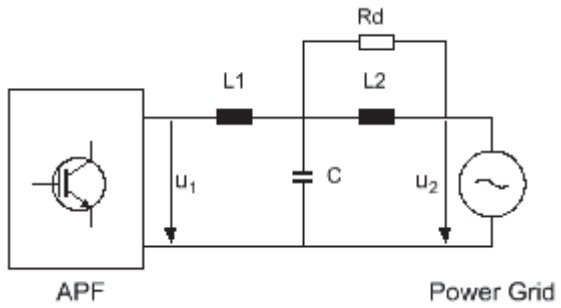

Figure 2: Parallel connection of the damping resistor.

Another aspect to be considered is the power dissipated by the damping resistor, because this power will be supplied to the interface filter by the inverter, which in turn, will absorb it from the power grid. It is obviously desirable that this power is minimal.

To determine the value of the constant k, the dependence between the active filtering performance and the damping resistor value was investigated, and as well, the influence on the dissipated power.

One of the most significant indicator of the filtering performance is the total harmonic distorsion factor of the current absorbed from the power grid with the active filter in operation.

It is noted that for values over 200 Ω, the total distorsion factor remains somewhat constant, because the damping resistance is mutch greater than the inductive reactance, losing its influence on the interface filter operation.

An optimal value from this point of view is 33Ω, under which, the total distorsion factor increases rapidly to unaccepable values.

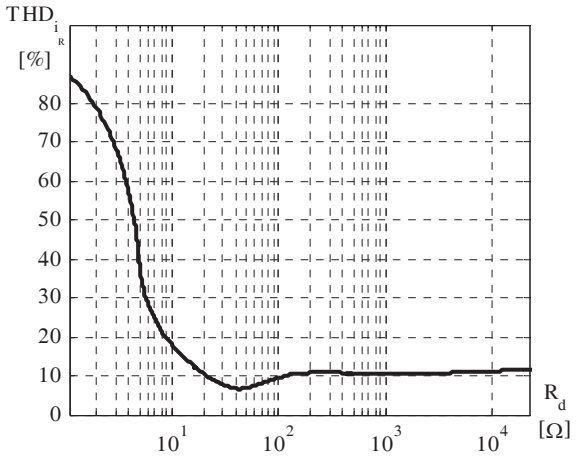

Figure 3: Compensated current THD versus parallel damping resistance.

To limit both losses and compensated current distorsion, a compromise between losses and current THD must be found. For thid purpose, figure 4 illustrates the dependence between the power dissipation and the damping resistance value.

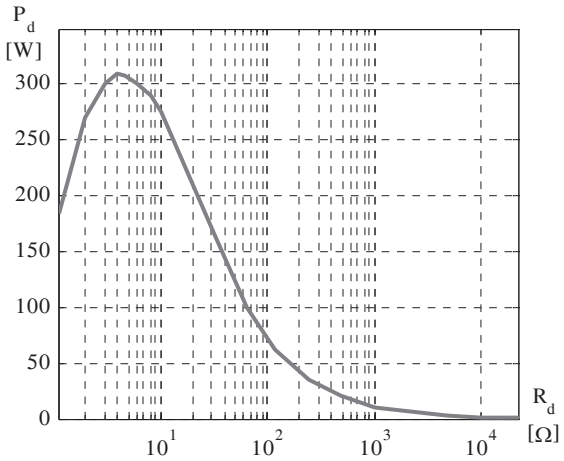

Figure 4: Power dissipation versus parallel damping resistance.

For the damping resistance optimum value of 33Ω, the power dissipation is about 163W, which makes the implementation difficult. At the same time, acceptable values for the losses involves unacceptable values for the current distorsion. Therefore, low cost implementation requires low power dissipation, that is, the range over 200Ω, where the damping resistance loses its effectiveness.

3.2. The series connection of the damping resistor

This time, the damping resistance is proportional to the capacitive reactance of capacitor C, which, at the resonance frequency takes again the value of 200Ω (fig 5).

The compensated current total harmonic distorsion factor dependence on the damping resistance, is illustrated in figure 6, which shows clearly a minimum at the resistance value of 330Ω.

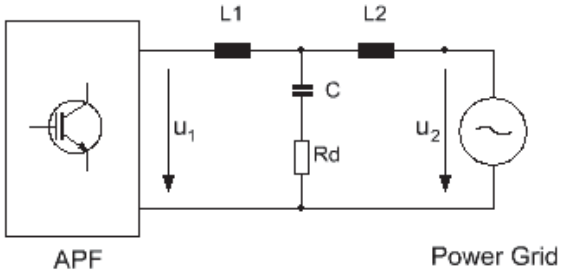

Figure 5: The series connection of the damping resistor.

For resistance values higher than 600 Ω, the compensated current total harmonic distorsion factor increases asymptotically to the value obtained whith the simpler, first order, interface filter.

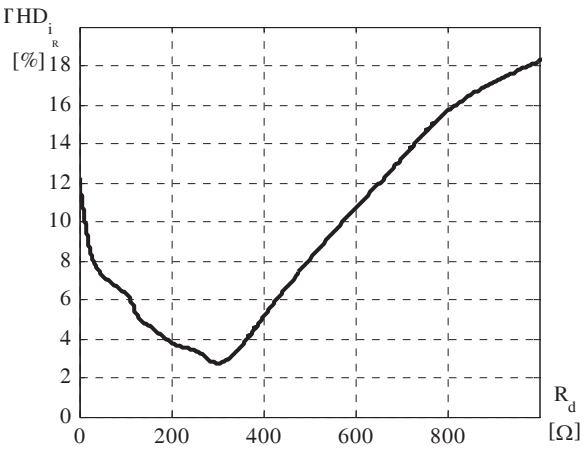

Figure 6: Compensated current THD versus series damping resistance

On the power dissipation, it has a low increase in the range between 22 and 270Ω, for the resistance value corresponding to the minimum current distorsion, the losses reach 46W, already being on the high slope.

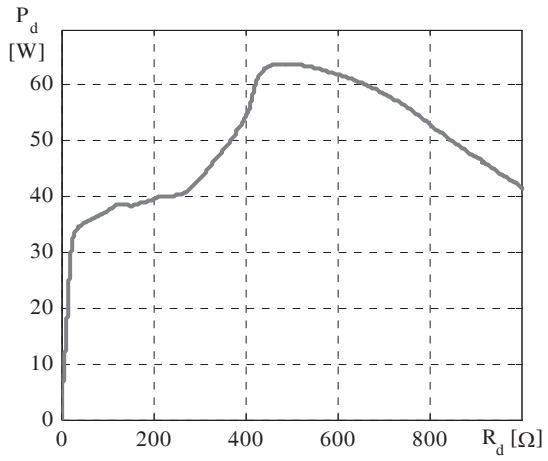

Figure 7: Power dissipation versus series damping resistance.

After exceeding the highest power dissipation, namely, for resistance values over 450Ω, the losses decrease slow and sure. This is because, when the damping resistance increases, the current through the capacitor decreases, and its contribution to the L_2C passive filter is reduced (and the current distorsion increases).

4. SWITCHING FREQUENCY LIMITATION. COMPENSATED CURRENT RIPPLE REDUCTION

The drawbacks due to the very low inductance L_1, should be treated differently, depending on the current control algorithm. Thus, for the hysteresis current controllers, the output current ripple is constant and equal to the hysteresis band, while the switching frequency depends on the instantaneous current value. When using PI controllers followed by PWM modulation, the switching frequency is constant and well-established , while the output current ripple is variable and dependent on external factors.

To limit the power inverter losses and also, the electromagnetic interference due to the high switching frequencies, for the first current control algortihm, a method for limiting the switching frequency was implemented.

For the case of PI controllers and PWM modulation, another method has been implemented, necesary to avoid instability due to oscillations of the comparators from the PWM modulator, applicable also for reducing the high current ripple due to the very low value of inductance L_1.

4.1. Using hysteresis current controllers

When using hysteresis controllers, the switching frequency is variable and dependent on many factors, therefore, to limit the maximum frequency, the dynamic of the filter output current should be limited. For this purpose, it was studied the loop feedback current filtration using low-pass filters. Since the feedback current applied to the loop will not coincide with the current passing the L_1 inductor, the output current should get „out of control". This however, does not happen, and the control system maintains a good response, in terms of compensated current distorsion, the better as the low-pass filter cutting frequency is higher (fig 8),but only with the damping resistors present in the interface filter.

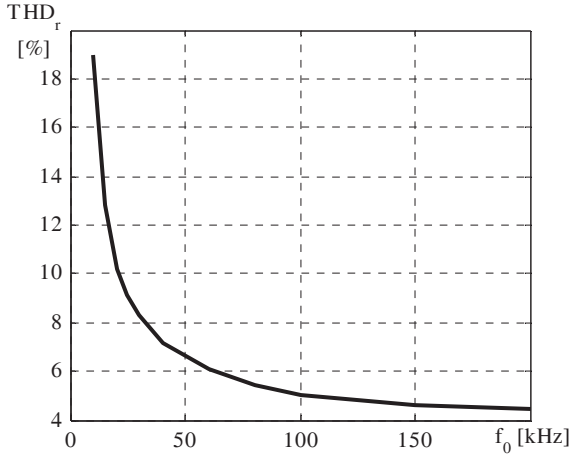

Figure 8: Compensated current THD versus cutting frequency of the low-pass filter.

Thus, the more the feedback current is smoothed, the more the maximum switching frequency is reduced (fig 9), but with negative effect on the compensated current distorsion, and on the damping resistors dissipated power, respectively, because the damping

resistors will limit large current variations through the first half of the interface filter.

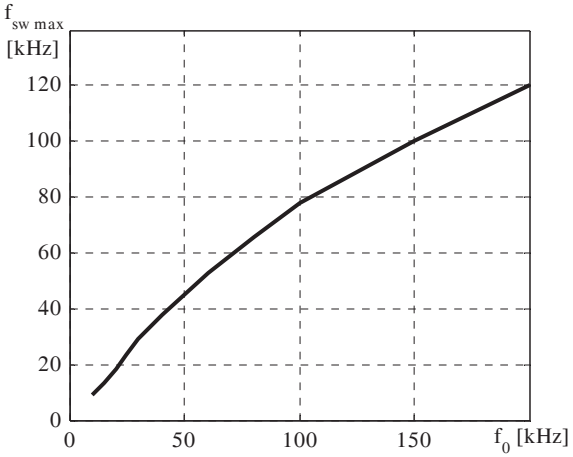

Figure 9: Inverter switching frequency versus low-pass filter cutting frequency.

Consequently, because the losses exceed 100W on all the low-pass filter cutting frequency range, the practical approach of this method could be very difficult. This is because resistors able to dissipate powers exceeding 100W are costly and their cooling is again difficult.

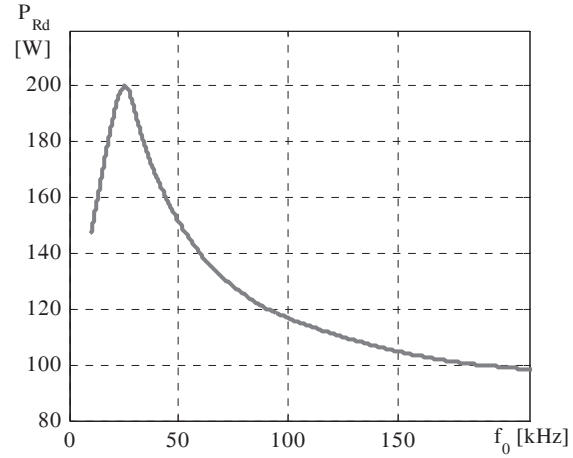

Figure 10: Damping resistor losses versus low-pass filter cutting frequency.

4.1. Using PI regulators and PWM carrier technique

In order to ensure a constant and low enough switching frequency not to endanger the power semiconductor devices of the active filter, is necessary to use a proportional-integrator regulator followed by a PWM modulator instead of the hysteresis regulator. Again, it is necessary to use a low-pass filter in the control loop, this time, to smooth the PI regulator output signal. This smoothing is necessary because the inverter side inductance is much to small to use a switching frequency of 20 kHz, as observed when using the hysteresis controller which resulted in a maximum switching frequency of 184 kHz. Thus, imposing a fixed switching frequency such as 15 kHz, would result in an output current through the inverter side inductor with a verry large ripple.

By simulation, however, it results in a different and strange behavior of the control system, namely, instead of the large output current ripple, important comparator oscillations occured. Specifically, due to the very rapidcurrent change through the inverter side inductor, and also, to the high speed of the PI controller, the PWM modulator input voltage, obtained at the controller output is „wrapped around" the triangular reference voltage, similar to the current tracking of the hysteresis regulator (fig 11-a).

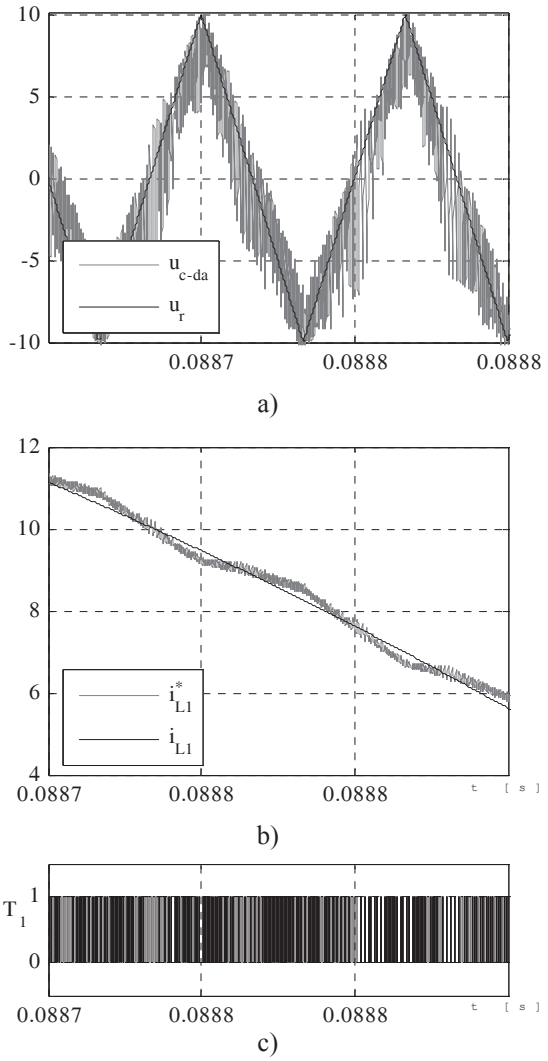

Figure 11: The PWM modulator operation when the comparator oscillations occur.

„Looking closer" at the gating signal for the inverter transistor, T_1, and using the Matlab Simulink environement facilities, the resulting switching frequency can be virtualy measured. Thus, although the switching frequency is imposed by the modulator carrier frequency to 15 kHz, in this particulary case,

its measured value is about 1.45 MHz. This value is the maximum switching frequency corresponding to the false hysteresis of the modulator control voltage, and after several simulations, it can be concluded that, the smallest the false hysteresis band, the higher the switching frequency, and the better the output current will follow the prescribed current, just as the system would be provided with a hysteresis current controller (fig 11-c; fig 12).

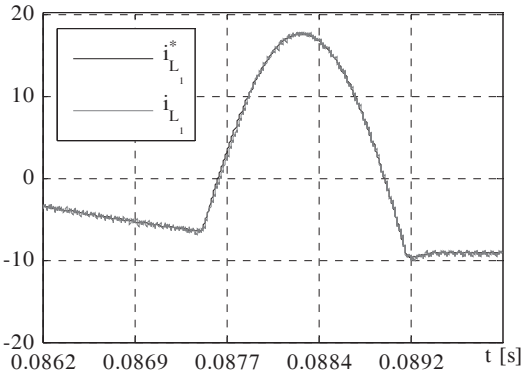

Figure 12: Prescribed current tracking when the comparator oscillations occur.

Another interesting phenomenon can be observed in figure 11-b, namely, if the unwanted high frequency switching is neglected, the output current is tracking the prescribed current with the frequency imposed by the carrier frequency, a behavior closer to the PWM modulation operation, but far from being a normal opration.

The major disadvantage of this event is the excessively high resulted switching frequency. Thus, although in terms of the output current, the results are avery good, the switching frequency can reach values as high as 3 MHz, which makes the use of PI controllers in this configuration, impossible.

After smoothing the output signal of the PI controller using low-pass filters, for a wide range of cutting frequencies, it can be concluded that smoothing the modulator input within certain limits, prevents the comparator oscillations and therefore, the correct opration of the system. In this respect, the behavior of the control system was studied for three carrier frequencies, of 10 kHz, 15 kHz and 20 kHz.

For the first studied carrier frequency, according to figure 13, it results in a cutting frequency range for the low-pass filter, between 15 and 30 kHz, for which, the system operation is correct and stable. Bellow the lower limit, the power transistors gating signals maintain a switching frequency of 10 kHz, but the situation appears when two successive pulses merge, so the switching frequency can no longer be considered to be constant. Over the upper limit, some local oscillations can appear, their appearance being more likely as the low-pass filter cutting frequency is higher. At the same time, the maximum abnormal switching frequency will be higher.

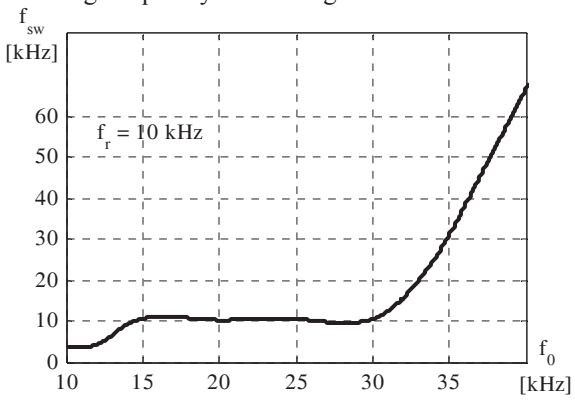

Figure 13: Switching frequency versus LPF cut-off frequency

In terms of total harmonic distorsion of the compensated current, only exceeding the lower limit is disavantageous, because the current distorsion increases with a steep slope (fig 14), otherwise, it slowly decreases with contant slope.

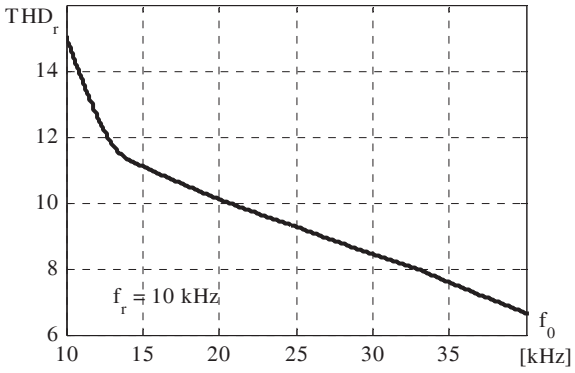

Figure 14: Compensated current THD versus LPF cut-off frequency

Since L_1 imposes a fast current variation at 10 kHz, the presence of the damping resistor is critical for current ripple reduction. And, at 10 kHz, the required „effort" is considerable, as seen in figure 15.

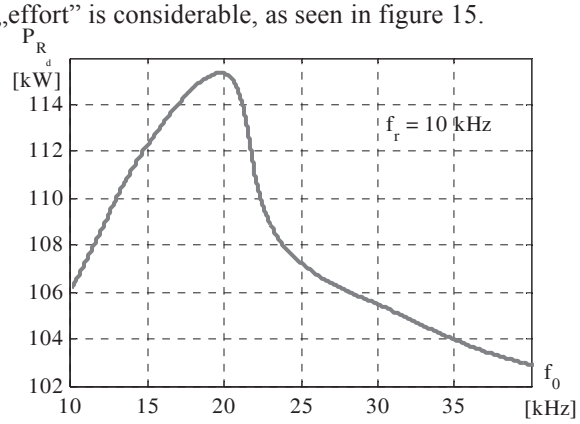

Figure 15: Damping resistance losses versus LPF cut-off frequency

Using a carrier frequency of 15 kHz, the low-pass filter cutting frequency range widens to 20 kHz, between about 20 and 45 kHz (fig 16).

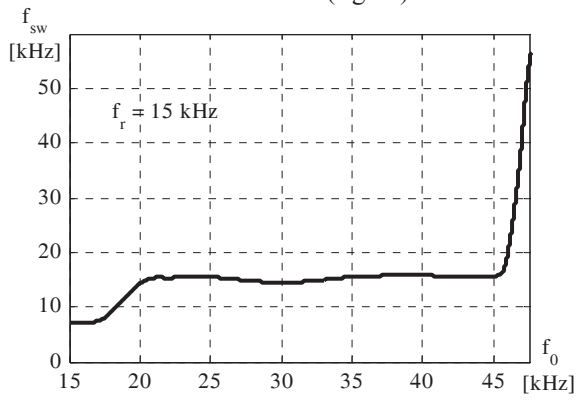

Figure 16: Switching frequency versus LPF cut-off frequency

Also, for this switching frequency, the current harmonic distorsion decreases at approximately constant slope, however, a slight saturation can be observed for high cutting frequencies, above the interval upper limit of about 45 kHz.

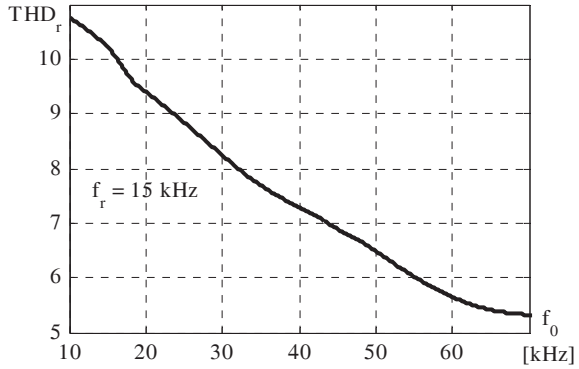

Figure 17: Compensated current THD versus LPF cut-off frequency

Due to the greater carrier frequency, the power dissipation on the damping resistance is lower than in the previous case, but still high.

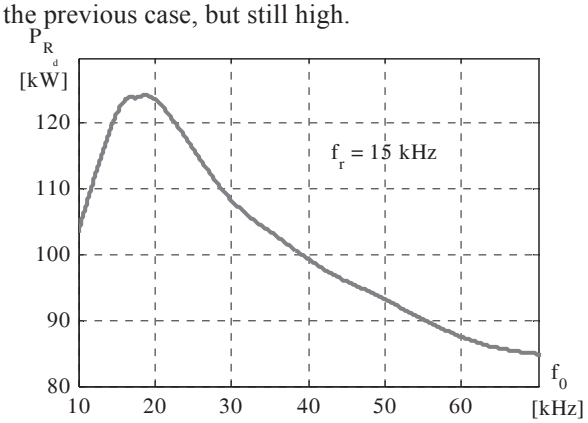

Figure 18: Damping resistance losses versus LPF cut-off frequency

A compromise between a sufficiently low switching frequency and a low power dissipated by the damping resistor is obtained for a carrier frequency of 20 kHz, when the cutting frequency range is even wider, of about 45 kHz (fig 19).

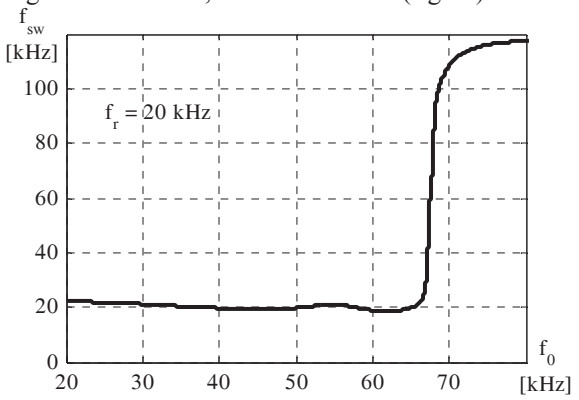

Figure 19: Switching frequency versus LPF cut-off frequency

For a low-pass filter cutting frequency of 60 kHz, the total harmonic distorsion factor of the compensated current is 5.91% (fig 20).

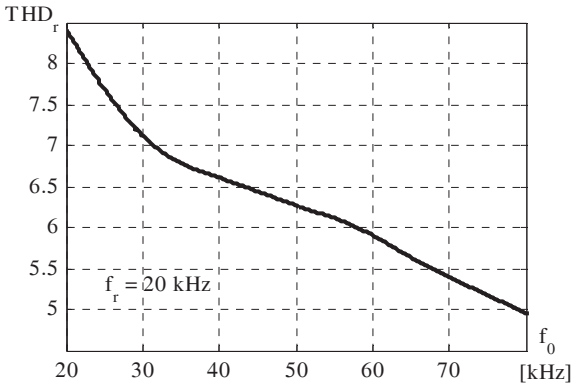

Figure 20: Compensated current THD versus LPF cut-off frequency

For the same operating point, the damping resistor losses are about 87W, which is below 100W for cutting frequencies above 40 kHz (fig 21).

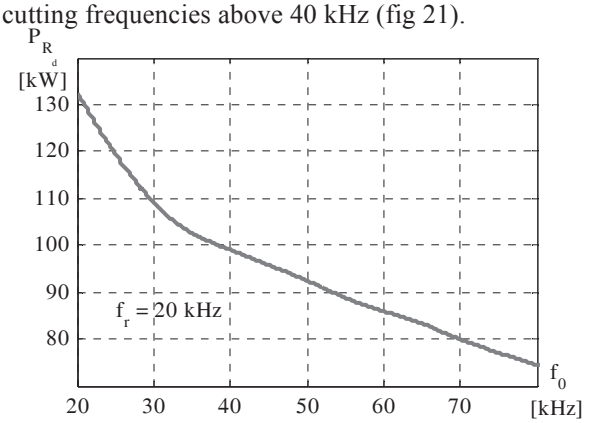

Figure 21: Damping resistance losses versus LPF cut-off frequency

From the three studied cases, it is found that with increasing carrier frequency, the cutting frequency range of sellection is widening, and also, the power dissipation on the damping resistor can be reduced by the use of a higher cutting frequency.

5. CONCLUSIONS

For this paper, multiple theoretical and experimental studies were accomplished, using a passive interface filter variant different from the existing literature. In this case, the 400 μH inverter side inductance is less than the grid side inductance and provides a very good dynamic response of the active filtration system, and also allows a higher performance of the interface filter. A drawback still remains against the implementation of the interface filter in this configuration, namely, the very high switching frequency resulted due to the very low inductance of the inverter side coil, which can get as high as 194 kHz.

To avoid the typical instability of this configuration, and the operation of the interface filter as a passive harmonics filter, the use of damping resistors was necesary. Conecting the damping resistor in series with the LCL filter capacitor, provides higher filtering performance and lower power dissipation, compared to mounting the resistor parallel to the grid side inductor. For example, a value of 200 Ω for the series damping resistance gives a compensated current harmonic distorsion of 3.85% and a dissipated power of about 40 W for the PI current control.

Due to the high switching frequency resulted for the hysteresis current controller, but also, to the PI current controller self-oscillating and instability, specific solutions where found to limit the switching frequency and to eliminate the instability, respectively. The found solutions give good results, but with the cost of increased damping resistor losses, because the resistor receives the role of limiting the additional curent variations through the inverter side inductor. The results show the advantages of the PI current control over hysteresis control, both in terms of active filtering efficiency and of practical implementation.

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